



# EV085425516

Application Number

First Named Inventor

Filing Date

M/2811

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**TRANSMITTAL** 

**FORM** 

PTO/SB/21 (08-00)

09/652,550

Keiji Jono

August 31, 2000

Approved for use through 10/31/2002. OMB 0651-0031

U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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#### 2811 Group Art Unit (to be used for all correspondence after initial filing) **Examiner Name** Q.D. Vu KM1-001 Attorney Docket Number Total Number of Pages in This Submission **ENCLOSURES** (check all that apply) After Allowance Communication Assignment Papers Fee Transmittal Form to Group (for an Application) Request, Appeal Communication to Board Drawing(s) Fee Attached Drawing(s) Red-lines, Formals Licensing-related Papers of Appeals and Interferences Appeal Communication to Group Amendment / Reply (Appeal Notice, Brief, Reply Brief) Petition After Final Proprietary Information Petition to Convert to a Provisional Application Affidavits/declaration(s) Status Letter Power of Attorney, Revocation Change of Correspondence Address Other Enclosure(s) (please identify below): Extension of Time Request Terminal Disclaimer Postcard **Express Abandonment Request** Request for Refund Information Disclosure Statement CD, Number of CD(s). Certified Copy of Priority NO FEES REQUIRED. Remarks Document(s) Response to Missing Parts/ The Commissioner is hereby authorized to charge any additional fees required under 37 CFR Sections Incomplete Application Response to Missing Parts 1.16 and 1.17 and credit any overpayments to: under 37 CFR 1.52 or 1.53 23-0925. SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT Reg. No. 40,045 D. Brent Kenady Firm WELLS ST. JOHN P.S. Individual name Signature Date

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EV085429516

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE,

Application Serial No. 09/652,550
Filing Date August 31, 2000
Inventor Keiji Jono et al.
Assignee KMT Semiconductor, LTD and Micron Technology, Inc.
Group Art Unit 2811
Examiner Quang D. Vu
Attorney's Docket No. KM1-001
Title: Methods of Forming an Isolation Trench in a Semiconductor, Methods of Forming an Isolation
Trench-Isolated Transistor, Trench-Isolated Transistor, Trench Isolation Structures
Formed in a Semiconductor, Memory Cells and DRAMS

# **RESPONSE TO NOVEMBER 6, 2002 OFFICE ACTION**

To:

Box Non-Fee Amendment

Assistant Commissioner for Patents

Washington, D.C. 20231

From:

D. Brent Kenady

Tel. 509-624-4276; Fax 509-838-3424

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Responsive to the Office Action dated November 6, 2002, Applicant amends and remarks as follows:

## **AMENDMENTS**

### In the Claims

Please replace the claims with the following clean version of the entire set of pending claims, in accordance with 37 CFR § 1.121(c)(1)(i). Cancel all previous versions of any pending claim.